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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,913	02/27/2004	Gi Hong Kim	DAE-0013	7507

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,913	KIM ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-17* is/are allowed.

6)☒ Claim(s) *1-9 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

1. Claims 1-18 are pending in the application.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it uses a phrase "Disclosed herein is" which can be implied. It is suggested that "Disclosed herein is" be deleted, and the remaining part of the first sentence be made into a complete sentence.

Correction is required. See MPEP § 608.01(b).

3. Claims 3 and 7 are objected to because of the following informalities:

Claim 3 recites "writing the data which is stored in the second sense amplifier in the step b)" which is unclear. In light of Fig. 6B, it will be understood as -- writing the data which is stored in the first sense amplifier in the step c)--.

Claim 7, in line 4, recites "the sense amplifier outside the memory block" which appears to lack antecedent basis, since "a sense amplifier of the memory block" in line 2 is of the

memory block and not outside the memory block. Therefore, "the sense amplifier" in line 4 will be understood as --a sense amplifier-- or --another sense amplifier--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Pat. No. 6,392,958) in view of Batson et al. (U.S. Pat. Appl. Pub. No. 2002/0067632).

Regarding claims 6 and 18, Lee discloses an SRAM-compatible memory, and a method of driving the SRAM-compatible memory, including a memory block (within 101) having DRAM cells arranged in a matrix form defined by rows and columns, the SRAM-compatible memory externally interfacing with an external system in which no timing period for performing a refresh operation is provided (inherent as an SRAM-compatible memory) and first and second external access periods (S_tRC in Fig. 2, for example, for any two access operations) are provided for externally accessing the SRAM-compatible memory, the first external access period including a first refresh period (for example, the RESERVE period in Fig. 2 used for a refresh operation, as implied in column 2, lines 22-25 and column 5, lines 21-23) and a first internal access period (the READ period in Fig. 2) and the second external access period including a second refresh period (same as the first external access period but for the second external access

period), the method comprising the steps of: a) fetching data to be refreshed from a DRAM cell in a first row of the memory block during the first refresh period (as a part of a REFRESH state operation; see column 5, lines 19-21); b) accessing a specified DRAM cell during the first internal access period (the READ period in Fig. 2); and c) rewriting the data fetched in the step a) in the DRAM cell in the first row of the memory block in the first refresh period (as a part of a REFRESH state operation; see column 5, lines 19-21).

Lee does not disclose that the rewriting step is executed in the second refresh period.

However, Batson discloses a dynamic content addressable memory (DCAM), which includes a DRAM array that needs refreshing, wherein a fetching step (a refresh-read operation) and a rewriting step (a refresh-write operation) of a refresh operation are executed in different access periods (i.e., different CAM search cycles; see for example paragraphs 0050 and 0051).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the Lee's memory and method by separating the refresh read operation (fetch) and the refresh write operation (rewrite) into two different external access periods, for the purpose of further reducing the time reserved for the refresh operation in a given external access operation of the Lee's SRAM compatible memory, thus increasing the access speed of the SRAM compatible memory.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-9 and 18 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3-5 of copending Application No. 10/810,749 ("Reference").

Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Regarding claims 1-7, claim 5 of Reference (along with parent claims) implies a method of driving an SRAM-compatible memory including memory blocks and sense amplifiers (the memory blocks and the sense amplifiers in claim 1 of Reference), the memory blocks each having DRAM cells arranged in a matrix form defined by rows and columns, the SRAM-compatible memory externally interfacing with an external system in which no timing period for performing a refresh operation is provided and first and second external access periods are provided for externally accessing the SRAM-compatible memory, the first external access period including a first refresh period and a first internal access period and the second external access period including a second refresh period (see claim 3 of Reference),

the method comprising the steps of: a) fetching data to be refreshed from a DRAM cell in a first row of a first memory block and storing the fetched data in a first sense amplifier during the first refresh period (as implied in claims 3-5 of Reference); b) storing the data fetched from

the DRAM cell in the first row of the first memory block and stored in the first sense amplifier in a second sense amplifier (the third sense amplifier in Reference; also implied in claims 3-5); and d) rewriting the data stored in the second sense amplifier (the third sense amplifier in Reference) in the DRAM cell in the first row of the first memory block during the second refresh period (implied in claims 3-5 of Reference).

However, Reference claims do not recite or imply the step of storing data to be read from or written to a DRAM cell in a second row of the first memory block in the first sense amplifier during the first internal access period in response to an address signal for selecting the second row, or reading the data stored in a sense amplifier outside the memory block during the first internal access period.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to store data to be read from or written to a DRAM cell in a second row of the first memory block in the first sense amplifier of Reference during the first internal access period in response to an address signal for selecting the second row (as a result of the external access of the second row) or to read the data stored in a sense amplifier outside the memory block during the first internal access period (i.e., in the second sense amplifier for the second memory block), since, as implied in claim 5 of Reference (after the third sense amplifier is disconnected from the first data lines), the first and second sense amplifiers of Reference are available to store desired data to be read from or written to the first and second memory blocks, respectively, including the second row of the first memory block or the second memory block which is "outside" the first memory block.

Regarding claims 8 and 9, claim 5 of Reference (along with parent claims) implies a method of driving an SRAM compatible memory including memory blocks and sense amplifiers (the memory blocks and the sense amplifiers, in claim 1 of Reference), the memory blocks each having DRAM cells arranged in a matrix form defined by rows and columns, the SRAM-compatible memory externally interfacing with an external system in which no timing period for performing a refresh operation is provided and first and second external access periods are provided for externally accessing the SRAM-compatible memory, the first external access period including a first refresh period and a first internal access period and the second external access period including a second refresh period (see claim 3 of Reference),

the method comprising the steps of: a) fetching first data to be refreshed from a DRAM cell in a first row of a first memory block and storing the fetched first data in a first sense amplifier (the third sense amplifier in Reference) during the first refresh period (implied in claims 3-5 of Reference); and c) rewriting the first data amplified by and stored in the first sense amplifier in the DRAM cell in the first row of the first memory block during the second refresh period (implied in claims 3-5 of Reference).

However, Reference claims do not recite or imply the steps of fetching second data from a DRAM cell in a first row of a second memory block and storing the fetched second data in a second sense amplifier during the first internal access period, and reading the fetched second data to an outside of the second sense amplifier.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to fetch second data from a first row of a second memory block and store the fetched second data in a second sense amplifier during the first internal access period, and to

read the fetched second data to an outside of the second sense amplifier, since, as implied in claim 5 of Reference (after the third sense amplifier is disconnected from the first data lines), the second sense amplifier of Reference is available to store desired data to be read from the second memory block, including the first row of the second memory block.

Regarding claim 18, claim 3 of Reference (along with parent claim 1) recites *inter alia* an SRAM-compatible memory device including a memory block having DRAM cells arranged in a matrix form defined by rows and columns, and externally interfacing with an external system in which no timing period is provided for performing a refresh operation of the DRAM cells (see parent claim 1 of Reference), wherein: first and second external access periods are provided for externally accessing the SRAM-compatible memory device, the first external access period including a first refresh period and a first internal access period, and the second external access period including a second refresh period; and the SRAM-compatible memory device performs an operation of fetching data from a DRAM cell to be refreshed during the first refresh period, and performs an operation of rewriting the data fetched during the first refresh period in the refreshed DRAM cell during the second refresh period (see claim 3 of Reference).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

8. Claims 10-17 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 10 and 16, the prior arts of record do not disclose or suggest an SRAM-compatible memory device as recited in claim 10 or 16, and particularly, a third switching unit for controlling an electrical connection between the first and second sense amplifiers.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Leung (U.S. Pat. No. 6,028,804) discloses an SRAM compatible memory.

Tang (U.S. Pat. No. 6,809,979) discloses an interleaved refresh operation.

Kim et al. (U.S. Pat. Appl. Pub. No. 2004/0233758) is a publication associated with the co-pending application No. 10/810,749.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7/11/05

Jung (John) Hur
Patent Examiner

jhh